What is claimed is:

1. A method of producing an integrated circuit die, said method comprising:

cutting a wafer from an ingot of substrate material;

forming a plurality of active integrated circuit patterns on one side of said wafer;

dividing said wafer into a plurality of individual dies wherein each die includes at least one perimeter edge, an inactive surface, an active surface including at least one of said circuit patterns thereon, and a layer of remaining substrate material on said at least one perimeter edge; and

removing a portion of said layer of remaining substrate material from said at least one perimeter edge of one or more of said integrated circuit dies.

2. The method of claim 1 wherein said step of removing is performed using the process of chemical mechanical planarization.

3. The method of claim 1 wherein said step of removing is performed by grinding away said portion of said layer of remaining substrate material.

4. The method of claim 1 further including the step of determining which of said dies are known good dies and subsequently subjecting said known good dies to the step of removing a portion of said remaining substrate material therefrom.

5. The method of claim 1 wherein said substrate material comprises gallium arsenide.

6. A method of producing an integrated circuit die, said method comprising:

cutting a wafer from an ingot of substrate material;

forming a plurality of active integrated circuit patterns on one side of said wafer;

determining which of said plurality of active integrated circuit patterns is a known good circuit;

dividing said wafer into a plurality of individual dies wherein each die includes at least one perimeter edge, an inactive surface, an active surface including at least one of said circuit patterns thereon, and a layer of remaining substrate material on said at least one perimeter edge;

selecting from said plurality of individual dies only known good dies having only one or more of said known good circuits thereon; and

removing a portion of said layer of remaining substrate material from said at least one perimeter edge of said known good dies.

7. The method of claim 6 wherein the step of removing further includes forming a bi-level step on said at least one perimeter edge.

8. An integrated circuit die cut from a wafer of substrate material, said die comprising:

an active surface having a circuit pattern formed thereon;

an inactive surface opposite said active surface;

at least one perimeter edge;

a layer of remaining substrate material on said at least one perimeter edge; and

wherein at least a portion of said layer of remaining substrate material is removed from said at least one perimeter edge of said integrated circuit die.

9. A known good integrated circuit die cut from a wafer of substrate material, said die comprising:

an active surface having a circuit pattern formed thereon;

an inactive surface opposite said active surface;

at least one perimeter edge;

a layer of remaining substrate material on said at least one perimeter edge; and

wherein at least a portion of said layer of remaining substrate material is removed from said at least one perimeter edge.

10. An integrated circuit assembly comprising a known good integrated circuit die formed from a wafer of substrate material and being mounted to a base, said die and said base encapsulated in a plastic material, wherein said known good integrated circuit die comprises;

an active surface having a circuit pattern formed thereon;

an inactive surface opposite said active surface;

at least one perimeter edge;

a layer of remaining substrate material on said at least one perimeter edge; and

wherein at least a portion of said layer of remaining substrate material is removed from said at least one perimeter edge.